TECHNIQUES FOR REDUCING LEAKAGE CURRENT IN ON-CHIP IMPEDANCE TERMINATION CIRCUITS

ABSTRACT OF THE DISCLOSURE

[0046] Techniques for reducing the leakage currents through on-chip impedance termination circuits are provided. An on-chip impedance termination circuit includes a network of resistors and transistors formed on an integrated circuit. The termination circuit is coupled to one or more IO pins. The transistors can be turned ON and OFF to couple or decouple subsets of the resistors from the IO pins. The bodies of transistors 305-306 are coupled to a supply voltage to cut off leakage current. By pulling the body of these transistors to a supply voltage, the transistor's drain/source-to-body diodes turn OFF preventing unwanted leakage current. Also, by moving the source/drain/body node of transistors 301-304 to Node 2, leakage currents through transistors 301-304 are eliminated.